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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,474	03/21/2005	Chee Yen Tee	SG02 0024 US	4373

65913 7590 10/11/2007

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EXAMINER	
KIM, HAROLD J	
ART UNIT	**PAPER NUMBER**
2181	

NOTIFICATION DATE	DELIVERY MODE
10/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,474	TEE ET AL.	
	Examiner	Art Unit	
	Harold Kim	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-6* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are presented for examination.

2. This application has been filed with drawings that are not properly labeled. For easier search for examiners in future, please label all of the boxes.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, and 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al., US Patent no. 7,058,747.

5. In re claim 1, Chang et al. shows an interface integrated circuit device [401, fig 4] for interfacing a USB connection [col 9, line 11] to a further circuit [col 9, lines 10-14], the interface integrated circuit comprising:

first external terminals [403, fig 4] for connecting to a USB bus;

a transceiver [413, 414, 401, fig 4] capable of transceiving for both a USB host [USB host, col 9, line 12] and a USB device [USB device, col 9, line 14], the transceiver having a USB interface [413, fig 4], a host interface [407, fig 4] and a device interface [408, fig 4], the USB interface being coupled to the first external terminals [403, 413, fig 4];

second external terminals [404, fig 4] coupled to the device interface for

connection to an external USB device controller [col 9, lines 12-14];

a host controller [409, fig 4] coupled to the host interface, the host controller having a parallel data/address bus [col 9, lines 50-53];

third external terminals [405, fig 4] coupled to the parallel data/address bus.

6. In re claim 3, Chang et al. shows an electronic apparatus with a USB connection [403, fig 4], the electronic apparatus comprising a functional circuit [col 8, lines 49-56] with a processor [410, fig 4], a parallel address data bus [col 9, lines 50-53] coupled to the processor and a USB device controller circuit [410, fig 4] with a USB interface [407, 408, fig 4] in parallel with said address/data bus, the apparatus comprising an interface integrated circuit [401, 414, fig 4] electronically between the USB connection on the one hand and the parallel address/data interface and the USB interface on the other hand, the interface integrated circuit comprising:

first external terminals [403, fig 4] for connecting to the USB connection;

a transceiver [413, 414, fig 4] capable of transceiving for both a USB host [USB host, col 9, line 12] and a USB device [USB device, col 9, line 14], the transceiver having a USB interface [413, fig 4], a host interface [407, fig 4] and a device interface [408, fig 4], the USB interface being coupled to the first external terminals;

the device interface being connected to the USB device controller circuit [410, fig 4] in said functional circuit [col 8, lines 49-56];

a host controller [409, fig 4] coupled to the host interface, the host controller being coupled to the processor via the parallel data/address bus [col 9, lines 50-53].

7. In re claim 4, Chang et al. shows the apparatus is arranged to use USB communication from said host controller via the USB connection in a first speed mode when operating as USB host and to use USB communication via the USB connection in a second speed mode, different from said first speed mode, as determined by the device controller when operating as USB device [col 8, line 65 to col 9, line 8].

8. In re claim 5, Chang et al. shows an electronic system [fig 4] comprising one or more USB bus connections [403, 404, fig 4], a host apparatus [USB host, col 9, line 12] and a device apparatus [USB device, col 9, line 14], at least one of the host and the device apparatus comprising a functional circuit with a processor [col 8, lines 49-56], a parallel address data bus [col 9, lines 50-53] coupled to the processor and a USB device controller circuit [410, fig 4] with a USB interface [407, 408, fig 4] in parallel with said address/data bus [col 9, lines 50-53], the apparatus comprising an interface integrated circuit [401, 414, fig 4] electronically between the USB connection on the one hand and the parallel address/data interface and the USB interface on the other hand, the interface integrated circuit comprising:

first external terminals [403, 404, fig 4] for connecting to a USB bus connection;

a transceiver [413, 414, fig 4] capable of transceiving for both a USB host [USB host, col 9, line 12] and a USB device [USB device, col 9, line 14], the transceiver having a USB interface [413, fig 4], a host interface [407, fig 4] and a device interface [408, fig 4], the USB interface being coupled to the first external terminals;

the device interface being connected to the external USB device controller circuit [410, fig 4];

a host controller [409, fig 4] coupled to the host interface, the host controller being coupled to the processor via the parallel data/address bus [col 9, lines 50-53].

9. In re claim 6. Change et al. show a method of operating an interface integrated in a USB system [fig 4], the method comprising:

receiving a selection whether the apparatus containing the interface integrated circuit should operate as a USB host or as a USB device [col 9, lines 9-19];

transceiving USB signals with a transceiver in the interface integrated circuit [413, fig 4];

sequencing USB communication via the transceiver with a host controller in the interface integrated circuit and communicating USB transceived data to or from functional circuits outside the integrated circuit via a parallel address data interface when USB host operation is selected [col 9, lines 20-53], and

passing USB signals from the transceiver to a device controller in the functional circuits outside the integrated circuit when USB device controller operation is required [col 9, lines 32-38].

10. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Further references of interest are cited on Form PLO-892, which is attachment to this office action.

Any response to this action should be mailed to:

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P.O. Box 1450
Alexandria, VA 22313-1450

The centralized fax number is 571-273-8300.

The centralized hand carry paper drop off location is:

U.S. Patent and Trademark Office
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Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application should be directed to the central telephone number (571) 272-2100.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Harold Kim whose telephone number is 571-272-4148. The examiner can normally be reached on Monday-Friday 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 or call 571-272-1000.

HK

Harold J. Kim
Patent Examiner
September 30, 2007/HK

10/1/07

SUPERVISORY PATENT EXAMINER